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Grid-Tied Photovoltaic for High-Efficiency Transformer-less MOSFET Inverter

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***Abstract*: This paper suggests the use of MOSFETs with the super-junction as the main power buttons as a new high performance transformer-free photovoltaic grid-tied inverter. For the main power switches, reverse recovery problems are not needed, and blocking voltages through the switches is half the DC input voltage of the topology proposed. Consequently, the MOSFET super junction was used to increase performance and PR and fuzzy logic controller are used to improve efficiency. The PV module will be disconnected from the grid at freewheel mode with two additional switches using traditional H-bridge topology. It minimizes the high-frequency common-mode (CM) voltage leading to leakage current. For the proposed topology PR and the fuzzy logic controller which reduces the distortion of the AC output current. PWM dead time is not necessary. The light-load efficiency is improved by the use of MOSFET as main switches, thereby improving the performance of the proposed topology in the European Union (EU). With its high efficiencies that require a low cooling system, the proposed inverter can also work at a high frequency. Computation and analysis of total losses of semiconductor systems in the proposed topology and several current topologies. The proposal actually MATLAB / Simulink program simulates new topology to test the theoretical description precision. It is generated to test the effects of the experiments.**

***Keywords*: Common-Mode (CM) Voltage, Leakage Current, Converter, European Efficiency, Grid Connected, High Efficiency, Photovoltaic (PV), Transformer-less, PR, and fuzzy logic controller.**

1. Introduction

Raise the interest in renewable energy sources in conjunction with environmental degradation is a result of increased demand for global power and rising prices for other energy sources. Many renewable sources of energy are now available; among them, PV is the most up-to-date technique for solving energy problems. Because of the PV module's large-scale manufacturing capability, Grid-connected PV inverters that consist of a line frequency transformer are wide in size; make the entire device extensive and hard to mount. It is also a daunting job to improve performance and cut costs by using a high-frequency transformer that needs several power stages. On the other hand, the advantages of lower cost, higher performance, smaller scale, and weight are transformer-less grid-tied inverters.Nonetheless, due to the absence of a transformer that creates a CM leakage current, there is a galvanic relation between the power grid and the PV module.This CM leakage current increases the grid current harmonics and device losses, as well as generates strongly induced and radiated electromagnetic interference.Numerous researchers from various countries have sought transformer-less grid-tied PV inverters, scope research. Most of the inverters mentioned in the literature and commercially available displayPR and fuzzy logic controller efficiency of 97 percent -98 percent for the European Union (EU). Consequently, multiple topologies were proposed to increase the performance of the transformer-less inverters by using MOSFETs as key switches. Super-junction MOSFETs will avoid the losses of fixed voltage and turn-off caused by the current at the neck. Yu et al. Proposed a MOSFET H6 type inverter by eliminating the use of low-competence IGBTs as shown in Fig.1 (a). The indicated H6 type inverter peak and EU efficiencies were 98.3 percent and 98.1 percent respectively on the 300W prototype circuit with 180V DC bus voltage and 30 kHz operating frequency. The grid current flows through three switches in the active mode of the H6 type MOSFET inverter, resulting in higher conduction losses still remaining. Another problem is that if a phase change occurs in the inverter output voltage and current the anti-parallel diodes of MOSFETs would be triggered. Accordingly, system efficiency is decreased due to problems with MOSFET anti-parallel diode reversal recovery.

GU et al. Proposed MOSFET inverter with high reliability and efficiency (HRE) as shown in Fig. 1(b).Transformer-less inverter efficiency can be implemented using MOSFET and SiC diodes super junction. The super junction MOSFETs will prevent the losses of fixed voltage and turn-off caused by the tail current, thereby reducing the losses of conduction and switching. Nonetheless, due to poor reverse recovery of slow body diode MOSFETs, it is restricted to use in transformer-less inverters. Based on their circuit structure, performance, and CM voltage clamping capability, MOSFET-based transformer-less topologies for grid-tied PV applications will be reviewed and discussed here. The highly effective and

stable inverter principle (HERIC) topology which is shown in Fig is the most attractive transformer-less topology. 1(1)(a). Some commercial inverters, particularly those from Sunway's converter, implemented this topology. Within the ac side of a full-bridge (FB) topology two switches are inserted to decouple the PV module from the grid during the freewheeling period. Although the PV module is decoupled from the grid, it may be possible to detect a fluctuating CM voltage because the freewheeling path potential is not clamped at half the dc input voltage. As seen in Fig. 1(b), the topology suggested in replaces the two freewheeling switches with one bidirectional switch and four diodes of topology called the HB-ZVR bridge zero-voltage rectifier. Furthermore, another diode (D5) was introduced to help remove the current leakage. This topology's clamping feature was performed using D5 which allows one-directional clamping only if the freewheeling path potential (VAN-like VBN) is higher than the midpoint dc-link voltage. As a result, fluctuation of the CM voltage may be observed when the reverse condition occurs which is very smaller than the topology of HERIC.

Over the entire grid cycle, the Grid current flows through two switches, resulting in a low driving loss. Fig. 1(c) reveals a specific topology called the H5 topology, which is composed of the addition of an extra switch on the FB dc side. Within this topology, the S1 and S3 body diodes flow during the positive half cycle and S3 and S1 during the negative half cycle. Consequently the S1 and S3 switches could not be used with MOSFETs because the MOSFET body diode was poor reverse recovery. Another downside is the three switches in active mode, which allow for higher conductive loss, to flow through the output current for the entire grid cycle. There may also be a fluctuating CM voltage, as the freewheeling path potentials are not clamped at the intermediate point of the dc connection. An extension of H5 topology was introduced in which an additional switch (S6) with H5 topology was inserted in order to clamp the voltage of CM at half the input voltage, as shown in Fig. 1(d) of the file. Regrettably, there needs to be additional dead time between the S5 and S6 switch gate signals to prevent the Cdc1 input split condenser shortcut. Consequently, in the dead phase, CM voltage fluctuates. Another drawback is that higher losses of conduction exist because of the grid current flows through three active mode switches. Another topology, named full bridge with dc bypass, which is also called H6 topology, was proposed by Gonzalez et al. There are two switches and two FB inverter diodes on the dc side. Since the two-dimensional clamping branch, the CM characteristics of this topology are different than other topologies.

Due to the fact that the freewheeling path potential is greater or less than half the dc connecting voltage during D1 and D2 can be conducted during the freewheeling mode, both diodes D1 and D2 can be conducted. In this topology, only the turning speed of the clamping diodes depends on the leak current removal effect. However, only two MOSFET switches (S5 and S6) can enforce this topology. Furthermore, the grid current flows over four switches, which results in higher conduction losses. Taking into account the benefits and drawbacks of the transformerless inverter described above, two asymmetrical phase legs of the paper suggest a new transformer-less topology for aPR and fuzzy logiccontroller single-phase PV device. The key features of the inverter are:

1) There is no time to die because all the switches in the same step leg have never been switched on during the same SPWM cycle; the distortion at the actual output is therefore smaller.
2) Because of the addition of the clamping branch, the cm voltage is preserved at the half input voltage dc,
3) The inductor current flows through two and three switches during the positive and negative half-cycles respectively, thereby raising the conductivity loss.

This paper outlines the detailed operating principles and the PR and fuzzy logic controlmechanism for reducing the injection of dc current. A survey was done to measure the power losses of the unit and compare them in detail with the topologies shown in the figure. 1. Ultimately, the suggested topology is verified by the experimental findings. Ultimately an experimental data-based comparison table showing the efficiency of the proposed topology was summarized.

For the transformer-free PV converters, the two main issues are:

1) No leakage current will occur from the inverter.
2) Increase performance across a broader variety of loads. To resolve these two key problems, this paper proposes a new topology of a single-phase PV transformer-free grid-connected inverter.

The main characteristics of the inverter described are:

1) There will be no deadline, since in the same process leg; the switches have never all switched on during the same SPWM period.
2) The isolation of the PV module from the grid in freewheeling mode, which decreases the CM leakage current, is guaranteed by two additional switches and two diodes.
3) Switching and lead losses are also of.

This paper explains the detailed operating theory of a three-level inverter using unipolar SPWM. For 20 kHz and 40 kHz switching frequencies, the proposed inverter is effectively measured in contrast.

2. Proposed Unipolar SPWM Modulated Converter

A. Circuit Configuration

Fig. 3(a) shows the proposed transformer-less PV inverter topology which consistsof six MOSFET switches (G1-G6) and two diodes (D1-D2). Switches G5 and G6 are commutates with the switching frequency to de-couple the converter from the grid in the freewheeling mode. LA, LB, and Co make up the LCL type filter connected to the grid. Vpvand Cdcrepresent the input voltage and the DC link capacitor.

Unipolar SPWM can employ to the proposed topologyPR and fuzzy logiccontroller with three-level output. The super-junction MOSFETs can be utilized in the proposed required in the proposed configuration of the inverter. Consequently, the efficiency of the entire PV system is increased.

B. Operating Principle of the Proposed Topology:

Grid-tied photovoltaic system generally operates at a unity power factor. Fig. 3(b) shows the waveform of the switching pattern for the proposed topology. As can be seen, (G1, G4) and (G2, G5) commutates at the switching frequency with the identical commutation order in the positive and negative half cycle of grid current, respectively. Four operation modes are proposed that generate the output voltage state of +VPV, 0, and –VPV. Fig. 3 shows the operating principles of the proposed topology, where VAN and VBN are the voltages of the full H-bridge inverter from mid-point A and B of the bridge leg to the reference point N.

1. Mode 1 is the active mode in the positive half cycle of the grid current. When G1 and G4 are turnedon, the voltage VAN = VPV and VBN = 0, thus VAB = V*PV* and the CM voltage,

$$V_{CM} = \frac{(V_{AN} + V_{BN})}{2} = \frac{V_{PV}}{2} \qquad (1)$$

2. Mode 2 is the freewheeling mode in the positive half cycle of grid current as indicated in Fig. 3(b). The freewheeling current flows through G6 and D2. In this mode, VAN = VBN = VPV/2, thus VAB = 0 and the CM voltage,

$$V_{CM} = \frac{(V_{AN} + V_{BN})}{2} \qquad (2)$$

Mode 3 is the active mode in the negative half cycle of grid current. Like as mode 1, when G2, G3, and G5 are turnedon, the voltage VAN = 0 and VBN = VPV, thus VAB = - VPV and the CM voltage,

$$V_{CM} = \left(\frac{V_{AN} + V_{BN}}{2}\right) = \frac{V_{PV}}{2} \qquad (3)$$

3. Mode 4 is the freewheeling mode in the negative half cycle of grid current. When G5 and G2 are turned-off, the freewheeling current flows through G3 and D1. In this mode,
VAN = VBN = VPV/2.
Thus VAB = 0 and the CM voltage,

$$V_{CM} = \frac{(V_{AN} + V_{BN})}{2} = \frac{V_{PV}}{2} \qquad (4)$$

As the analysis above, the CM voltage remains constant during the four commutation modes of the proposed inverter and equals to VPV/2. As a result, the inverter is hardly to generate CM leakage current. Furthermore, the blocking voltages across all switches are half of the DC bus voltage; thus, the switching losses are reduced significantly.

3. Power Device Losses And Efficiency CalculationAnd Comparison With Several ExistingTopology.

It is difficult to estimate the total power device losses in the power electronic circuit for predicting the maximum efficiency. In this section, the power losses by the switches of the proposed topology and the topologies proposedare calculated with the same circuit parameters given in TABLE I. It is necessary to take into account that the calculation of the losses is based on theory and its accuracy depends on the device datasheet accuracy.

4. Leakage Current Analysis And Power Devices Loss Calculation

A. Leakage Current Analysis for the Proposed Topology

The PV module generates an electrically chargeable surface area which faces a grounded frame. In the case of such configuration, a capacitance is formed between the PV module and the ground. Since this capacitance occurs as an undesirable side effect, it is referred to as parasitic capacitance. Due to the loss of galvanic separation between the PV module and the grid, a CM resonant circuit can be created. An alternating CM voltage that depends on the topology structure and control scheme can electrify the resonant circuit and may lead to high ground leakage

B. Loss Reduction by Replacing IGBTs with MOSFETs as Main Power switches for the Proposed Topology

In this section, loss reduction by replacing IGBTs with MOSFETs as main power switches for the proposed topology is investigated to highlight the benefit of super-junction MOSFETs.
The total semiconductor power device losses in the proposed topology by using MOSFETs and IGBTs as main power switches are calculated at different EU output power with 20 kHz and 40 kHz operating frequencies which areillustrated in Fig. 6. It is clear that the total power device

C. Power Devises Loss Calculation and Comparison

In this section, the device power losses for the H5, HERIC, H6, oH5, and proposed topologies are calculated for 5-kW rated power with the same circuit parameters given in Table III. It is necessary to take into account that the calculation of the losses is based on theory and its accuracy depends on the device datasheet accuracy. In Table, I, the device type and their voltage stress, and distribution of the device number for different types of lossesare given. It can be seen that the devices for switching loss for all the topologies are the same but the other losses are different. The lowest conduction loss would be observed for HERIC topology as grid current flows only two switches, while the proposedtopology takes place second position. However, it is noticeable that the zero-vector conduction loss of MOSFET + SiC diode freewheeling path for the proposed topology is less than the IGBT + body-diode freewheeling path of the HERIC, H5, H6, and H5 topologies.

the topologies have been implemented with the unipolar SPWM technique with a three-level output voltage as +*V*PV,0, and -*V*PV, and alsoidentical filter inductor and capacitor values have been used; therefore, the losses across the output filter will be same for all the topologies which are neglected in this loss comparison. It can be seen that HERIC topology is with the least device loss, and the H5 and H6 topologies have the highest device loss as expected, while thePR and fuzzy logiccontroller proposed topology is in the second position.

1) Mode 1 is the active mode in the positive half cycle of the grid current. When S1 and S4 are turnedon, the inductor current *iL*increases linearly through the grid. In this mode, *V*AN = *V*PV and *V*BN = 0, thus *V*AB = *V*PV and the inductor current .

2) Mode 2 is the freewheeling mode in the positive half cycle of the grid current, as indicated in Fig. 5(b). The inductor current *iL*flows through S6 and D2 and reduces linearly under the effect of grid voltage. In this state, *V*AN falls and *V*BN rises until their values are equal. If the voltages (*V*AN≈ *V*BN) are higher than half of the dc-link voltage, freewheeling current flows through S7and D3 to the midpoint of the dc-link results in*V*AN and *V*BN are clamped at *V*PV/2. Therefore, at mode 2, *V*AN =*V*PV/2, *V*BN = *V*PV/2, the inverter output voltage *V*AB = 0 and the inductor current.

3) Mode 3 is the active mode in the negative half cycle of grid current. Similar to mode1, when S2, S3, and S5 are turned on, the inductor current increases in the opposite direction.In this mode, the voltage *V*AN = 0 and *V*BN = *V*PV, thus
*V*AB = -*V*PV and the inductor current.

4) Mode 4 is the freewheeling mode in the negative half cycle of grid current. When S5 and S2 are turnedoff, the inductor current flows through S3 and D1. Similar to mode2, if the voltages (*V*AN≈ *V*BN) are higher than half of the dc-link voltage, freewheeling current flows through S7and D3 to the midpoint of the dc-link, results in the voltages *V*AN and *V*BN are clamped at *V*PV/2. In this mode, *V*AN = *V*BN = *V*PV/2,*V*AB = 0, and the inductor current *iL*(*t*) = -*vgL*(*t*)(4)

As described above, the freewheeling path potential is clamped at the midpoint of the dc-link during the freewheeling period of the positive and negative half cycle. As a result, the inverter hardly generates any leakage current. It can also be seen that the anti-parallel diodes of the MOSFETs remained inactive during the whole operation period. Therefore, the proposed topology could be implemented utilizing MOSFET switches. However, the body diode will be activated if a phase shift occurs in the inverter output voltage and current. Accordingly, the dependability of the system will be reduced because of the MOSFET anti-parallel diode low reverse-recovery issues.

In the case of the transformer-less inverter, dc current injection into the utility grid is an important issue that may cause saturation of distribution transformer, increased loss, and abnormal operation of the load connected to the grid. In order to suppress the dc current injection into the utility grid, based on the control technique an improved control strategy, as depicted in Fig. 6, is implemented to control the proposed topology. The control block consists of a dc suppression loop, a grid current controller, and a phase-locked loop to synchronize with the grid current. The dc suppression loop is composed of a differential amplifier.

The transfer functions are given below:

$$G_{PR}(S) = K_{pi} + K_{ii}\frac{s}{s^2 + w_f^2}$$

$$G_d(s) = \frac{1}{1 + 1.5T_s s}$$

$$G_{PI}(s) = K_{pdc} + K_{idc}\frac{1}{s}$$

Where *K*pi and *K*ii are the proportional and resonant gain of the current controller, *K*pdc and *K*idc are the proportional and integral gain of the offset voltage controller, *ω*f is the fundamental frequency and *Ts*is the sampling period. Since an *LC* filter (*LCf*) has been used as an output filter; thus the system at the ac side can be described as follows:

$$\frac{di_g(t)}{dt} = \frac{v_{AB(t)}}{L} - C_f\frac{d^2v_g(t)}{dt^2} - \frac{v_g(t)}{L}$$

In the Laplace domain, (8) can be rewritten as

$$I_g(s) = \frac{V_{AB}(s)}{L_s} - C_f s^2 V_g(s) - \frac{V_g(s)}{L_s}$$

Where *Ig*and*vg* is grid current and voltage, and *V*AB is the inverter output voltage. Consequently, the equivalent model of the output filter can be drawn as Fig. 8.Henceforth, according to the above illustration, the overall control diagram can be depicted as shown in Fig. 11, where *G*dc(*s*) is the feedback gain of the dc suppression loop.

D. Fuzzy Logic Controller

FLC is one of the most successful operations of the fuzzy set theory. Its chief aspects are the exploitation of linguistic variables rather than numerical variables. FL control technique relies on human potential to figure out the system's behavior and is constructed on quality control rules. FL affords a simple way to arrive at a definite conclusion based upon blurred, ambiguous, imprecise, noisy, or missing input data. The basic structure of an FLC is represented in Fig 12.

- A Fuzzification interface alters input data into suitable linguistic values.
- A Knowledge Base which comprises of a database along with the essential linguistic definitions and control rule set.
- A Decision Making Logic which collects the fuzzy control action from the information of the control rules and the linguistic variable descriptions.
- A Defuzzification interface which surrenders a non-fuzzy control action from an inferred fuzzy control action

5. RESULTS

Leakage Current Analysis for the Proposed Topology: The PV module creates a surface with an electrically charged base. A capacitance is generated between the photovoltaic module and the soil in this case. This capacitance is called parasitic capacitance because it is an unwanted side effect. A CM resonant circuit can be formed due to the loss of the galvanic separation between the PV module and the grid. An alternate CM voltage depending on the topology configuration will electrify the resonant circuit and result in high ground leakage. In order to analyze the CM characteristics, an equivalent circuit of the proposed topology as shown in Fig. 16 can be drawn, where *V*AN, and *V*BN are the controlled voltage source connected to the negative terminal N, *L*CM and *C*CM are the CM inductor and capacitor, *C*P V*g*is the parasitic capacitance, and *Zg*is the grid impedance. According to the definition of CM and differential-mode (DM) voltage

$$V_{\mathrm{CM}} = \frac{1}{2}(V_{\mathrm{AN}} + V_{\mathrm{BN}}) \qquad (10)$$

$$V_{\mathrm{DM}} = V_{\mathrm{AN}} - V_{\mathrm{BN}} \qquad (11)$$

Where,*V*CM and *V*DM are, respectively, the CM and DM voltages. Solving (10) and (11),*V*ANand*V*BN can be expressed as follows:

$$V_{\mathrm{AN}} = V_{\mathrm{CM}} + \frac{1}{2}V_{\mathrm{DM}} \qquad (12)$$

$$V_{\mathrm{BN}} = V_{\mathrm{CM}} - \frac{1}{2}V_{\mathrm{DM}}. \qquad (13)$$

In order to illustrate the CM model at switching frequency, have been replaced for the bridge leg in Fig. 18.The grid is a low-frequency (50–60 Hz) voltage source; thusthe impact of the grid on the leakage current can be neglected.The DM capacitor *Co* can also be removed since it has no effect on the leakage current.

Consequently, the simplified high-frequency CM model of the proposed topology could be drawn as Fig. 17. The equation for the total CM voltage can easily be derived from Fig. 11 as

$$V_{t\mathrm{CM}} = V_{\mathrm{CM}} + \frac{V_{\mathrm{DM}}}{2}\frac{L_B - L_A}{L_A + L_B} \qquad (14)$$

Where *Vt*CM represents total CM voltage.Finally, the simplified single-loop CM model of the proposed.

Power Devises Loss Calculation and Comparison: In this section, the device power losses for the H5, HERIC,H6, H5, and proposed topologies are calculated for 5-kW rated power with the same circuit parameters given in Table III. It is necessary. In Table, I, the device type and their voltage stress, and distribution of the device number for different types of losses are given.It can be seen that the devices for switching loss for all the topologies are the same but the other losses are different. The lowest conduction loss would be observed for HERIC topology as grid current flows only two switches, while the proposed topology takes place second position from in fine on with the model The total power device losses at different output power for the H5, HERIC, H6, oH5, and proposed topologies are which are given in Table II and shown as a histogram in Fig. 19. The calculation process and the theories are studied, but not the contribution of this paper. Since all of the topologies have been implemented with the unipolar SPWM technique with a three-level output voltage as +*V*PV, 0, and -*V*PV, and also identical filter inductor and capacitor values have been used; therefore, the losses across the output filter will be same for all the topologies which are neglected in this loss comparison. It can be seen that HERIC topology is with the least device loss, and the H5 and H6 topologies have the highest device loss as expected, while the proposed topology is in the second positionswitches S1, S4, and S6.at 5-kW output power which validate the theoretical analysis.

Compared with the HERIC, the proposed topology increases the conduction losses and reduces the freewheeling losses as shown in Fig. 20. As a result, the total device loss for the HERIC topology at low power is higher than the proposed topology. On the other hand, the proposed topology cuts the conduction Fig.

6. Table

Inverter parameter	Value
Input voltage	400VDC
Grid voltage/ Frequency	230V/50Hz
Rated power	500w
AC output current	21.1A
Switching Frequency	20Hz

Table I. Parameters for Loss Calculation

	Total power device losses (W)				
Output Power (W)	H5 topology	HERIC topology	H6 topology	oH5 topology	Proposed topology
5000	75.0066	55.3325	94.6806	78.05	63.032
2500	27.7356	20.4257	35.0454	29.2573	22.3915
1500	14.5659	10.7865	18.3452	15.4789	11.245
1000	9.2108	6.8934	11.5282	9.8195	6.7667
500	4.6755	3.6179	5.7331	4.9798	3.0184
250	2.7153	2.2117	3.2188	2.8674	1.4179

Table II. Calculated Devices Total Power Loss

Inverter parameter	Value
Input voltage	400VDC
Grid voltage/Frequency	230v/50Hz
Rated power	1000W
AC output current	4.1 A
Switching Frequency	20KHz
DC bus capacitor	470microF
Filter inductor La,Lb	2mF
Filter capacitor	2microF

PV parasitic capacitor Cpv1,Cpv2	75nF

Table III. Parameters used in Simulation

PR and Fuzzy Grid currentTHD	**0.96**
PI and PR Grid current THD	**1.81**

Table IV. Results of PI and PR controller.

7. Figures

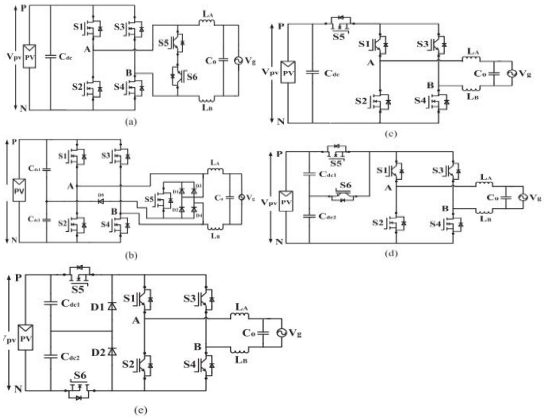


Fig 1: Some existing MOSFET-based transformerless topologies for grid-tied PV application: (a) HERIC topology (b) HB-ZVR topology (c) H5 topology (d) H5 topology (e) H6 topology

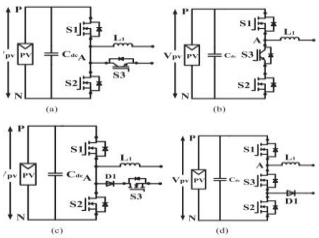


Fig 2: MOSFET-based phase legs for a transformerless inverter: (a) HERIC method (b) H5 method (c) Modification of a HERIC method (d) Modification of an H5 method.

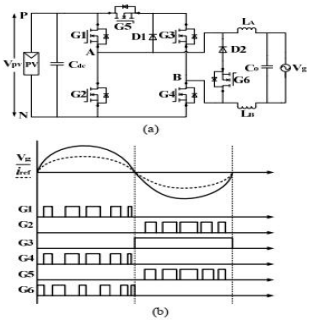


Fig 3: Proposed transformer-less grid-connected PV inverter (a) Structure of the converter (b) Gate drive signals

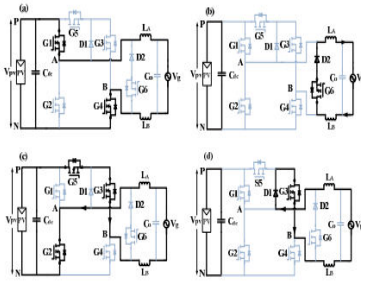


Fig 4: Operation principle of the proposed topology

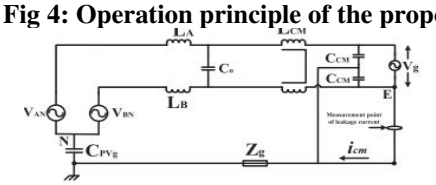


Fig 5: Equivalent CM model of the proposed topology

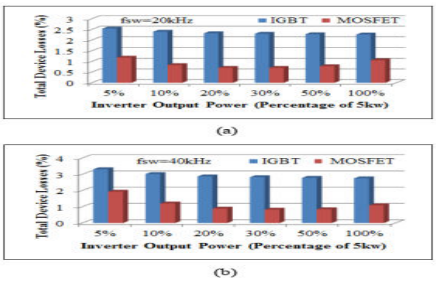


Fig 6: Total device losses for the proposed topology by employing IGBTs and MOSFETs as power switches (a) 20 kHz operating frequency (b) 40 kHz operating frequency.

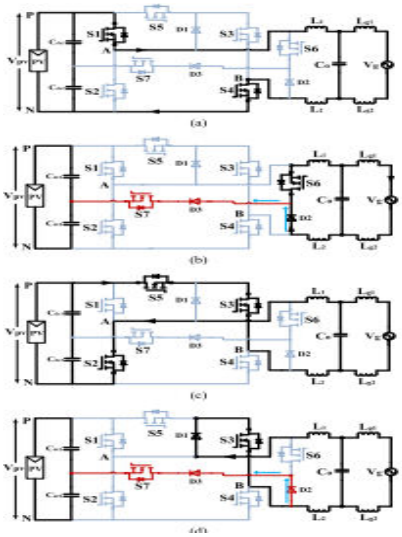


Fig 7: Operating principle of the proposed topology: (a) Active and (b) freewheeling modes in the positive half cycle of the grid current, (c) active, and (d)freewheeling modes in the negative half cycle of the grid current.

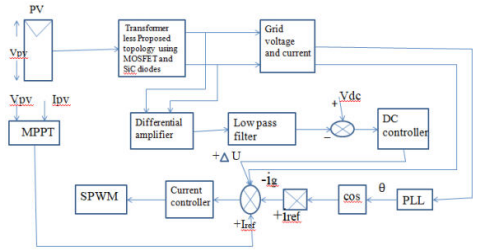


Fig 8: Control block of the proposed topology

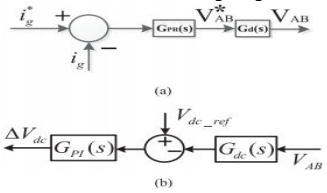


Fig 9: (a) Block diagram of the PR controller. (b) Block diagram of the dc suppression loop

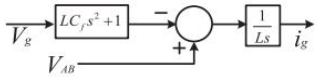


Fig 10: Equivalent model of the output filter in a Laplace domain

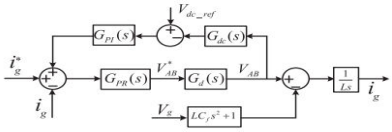


Fig 11: Block diagram of PR

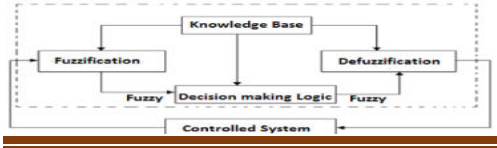


Fig 12: Basic structure of a Fuzzy Logic controller

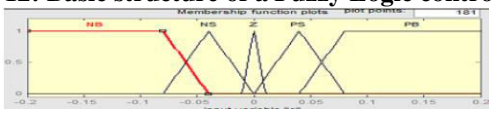


Fig 13: Error as input.

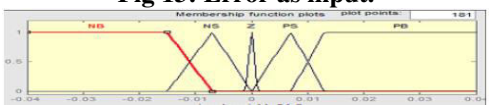


Fig 14: Change in Error as input.

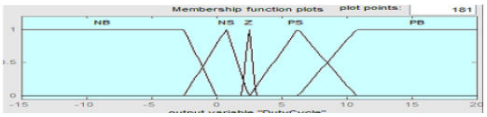


Fig 15: Output variables to the defuzzification process

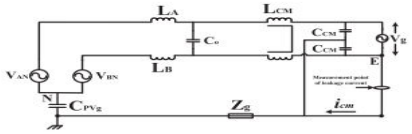


Fig 16: Equivalent CM model of the proposed topology

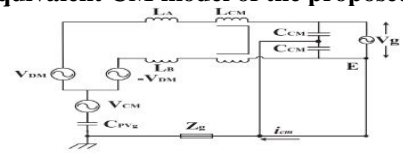


Fig 17: Simplified CM model at switching frequency.

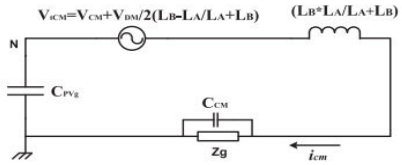
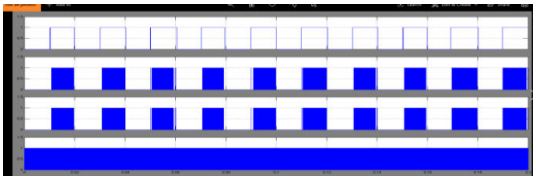


Fig 18: Simplified single-loop CM model.



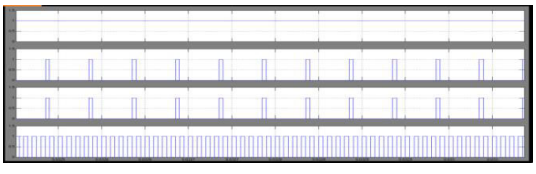


Fig 19: Experimental gate signals of the switches S1, S4, S6, and S7 (a) Grid cycle (b) PWM cycle.

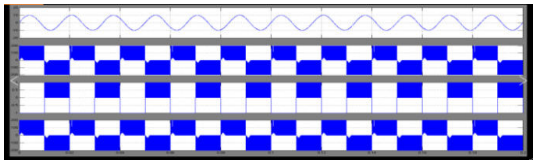


Fig 20: drain-source voltage waveform

Compared with the HERIC, the proposed topology increases the conduction losses and reduces the freewheeling losses as shown in Fig. 20. As a result, the total device loss for the HERIC topology at low power is higher than the proposed topology. On the other hand, the proposed topology cuts the conduction Fig.

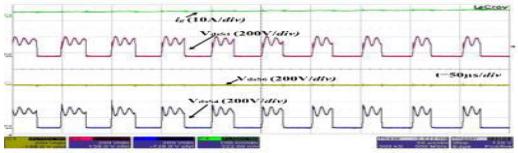


Fig 21: Enlarged view of the drain-source voltage waveform of the switches S1, S4, and S6.

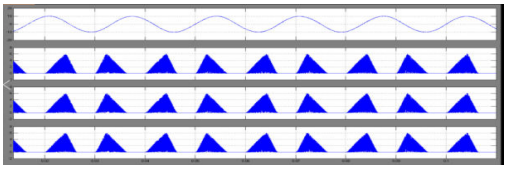


Fig 22: Current stress on the switches S1, S4, and S6.and freewheeling losses if compared with the H5, H6, and oH5topologies.

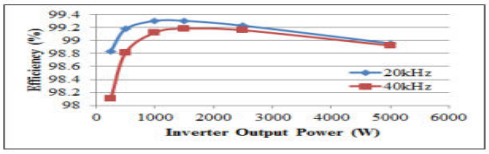


Fig 23: Efficiency of the proposed topology with 20 kHz and 40kHzswitching frequencies.

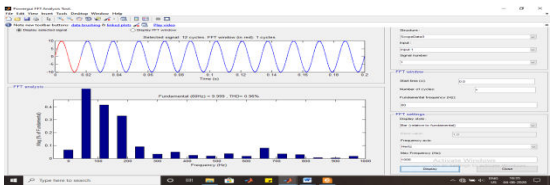


Fig 24: PR and fuzzy logic controller Grid current THD (Ig) =0.96

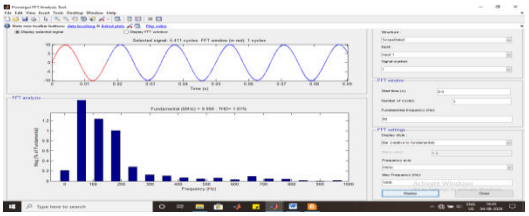


Fig 25: PI and PR controller Gridcurrent THD (Ig) =1.81

8. Conclusion.

A new transformer-free grid-mounted inverter is introduced in this article.PR and fuzzy logic controller. The key advantages of the topology suggested are:

1. MOSFETs may be used as main power switches because their antiparallel diodes are inactive to achieve high efficiency over a wide load range.
2. In all operating modes, CM mode voltage stays constant so the leakage current is well suppressed.
3. With the unipolar SPWM, perfection in differential mode is achieved.
4. The distortion of output current is lower as PWM dead time for the proposed topology is not needed.
5. With high working frequency, the proposed inverter will operate, while maintaining high performance, to minimize the output filter size.The proposed topology PR and the fuzzy logic controllerhasbeen MATLAB/Simulinksoftwareto verify the results. As a conclusion, the proposed inverter isenormously suitable for single-phase grid-tied PV application

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